



Thyristor Module

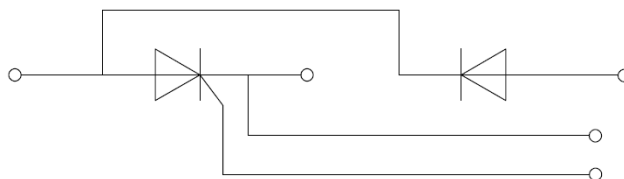
Features

- Half-bridge configuration with integrated SCR and diode in a single package
- High-thermal-conductivity DBC insulation for excellent heat dissipation
- Vacuum soldering technology for enhanced reliability

Applications

- Heating control
- Light control system
- DC motor

Parameter	Value	Unit
V_{RRM}	1800	V
$I_{T(AV)}(@ T_C = 85^{\circ}C)$	40	A
$I_{TSM}(@ t_p = 10ms)$	800	A
$V_T(Max)$	1.80	V



Absolute Maximum Ratings (@ $T_C = 25^{\circ}C$ unless otherwise specified)

Parameter	Conditions	Symbol	Values	Unit
Repetitive peak off-state voltage	$T_vj = 25^{\circ}C$	V_{DRM}	1800	V
Repetitive peak reverse voltage	$T_vj = 25^{\circ}C$	V_{RRM}	1800	V
Non-repetitive peak off-state voltage	$T_vj = 25^{\circ}C$	V_{DSM}	1900	V
Non-repetitive peak reverse voltage	$T_vj = 25^{\circ}C$	V_{RSM}	1900	V
Average forward current	$T_C = 85^{\circ}C$	$I_{T(AV)}$	40	A
Forward surge current	1/2 cycle, Sine wave, 50Hz $T_vj = 25^{\circ}C$	I_{TSM}	800	A
I^2t value for fusing		I^2t	3200	A^2s
Critical rate of rise of on-state current	$I_G = 2 \times I_{GT}$	di/dt	150	$A/\mu s$
RMS isolation voltage	A.C 50Hz(1s/1min)	V_{ISO}	3600/3000	V
Junction temperature range		T_J	-40 ~ +125	$^{\circ}C$
Storage temperature range		T_{stg}	-40 ~ +125	$^{\circ}C$

**Electrical Characteristics (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)**

Parameter	Conditions	Symbol	Values			Unit
			Min.	Typ.	Max.	
Peak forward voltage	$I_T=120\text{A}$, $t_P=380\mu\text{s}$	V_T			1.80	V
Repetitive peak off-state current	$V_D = V_{\text{DRM}}$, $T_{vj} = 25^\circ\text{C}$	I_{DRM}			100	μA
	$V_D = V_{\text{DRM}}$, $T_{vj} = 125^\circ\text{C}$				30	mA
Reverse leakage current	$V_R = V_{\text{RRM}}$, $T_{vj} = 25^\circ\text{C}$	I_{RRM}			100	μA
	$V_R = V_{\text{RRM}}$, $T_{vj} = 125^\circ\text{C}$				30	mA
Threshold voltage	For power loss calculation only $T_{vj} = 125^\circ\text{C}$,	V_{TO}			0.94	V
Dynamic resistance	$T_{vj} = 125^\circ\text{C}$,	r_T			4.5	$\text{m}\Omega$
Triggering gate current	$V_D=12\text{V}$ $R_L=30\Omega$	I_{GT}	20		120	mA
Holding current	$I_T=1\text{A}$	I_H			250	mA
Latching current	$I_G=1.2 I_{\text{GT}}$	I_L			300	mA
Critical rate of rise of voltage	$V_D=2/3V_{\text{DRM}}$ $T_{vj}=125^\circ\text{C}$ Gate Open	dv/dt	1000			$\text{V}/\mu\text{s}$
Triggering gate voltage	$V_D=12\text{V}$ $R_L=30\Omega$	V_{GT}			1.8	V
Non triggering gate voltage	$V_D=0.5V_{\text{DRM}}$ $T_{vj}=125^\circ\text{C}$	V_{GD}	0.25			V

Thermal Characteristics (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Conditions	Symbol	Values			Unit
			Min.	Typ.	Max.	
Thermal resistance, junction to case	per Thyristor	$R_{\text{th(j-c)}}$		0.65		K/W
Thermal resistance, case to heatsink	per Thyristor	$R_{\text{th(c-s)}}$		0.32		K/W
Mounting torque	Module and heatsink fixed torque M5	M	4.25		5.75	$\text{N}\cdot\text{m}$
	Electrode connection torque M5		2.55		3.45	$\text{N}\cdot\text{m}$



Ordering Information

Device	Marking	Package	Weight	Inner Box	Per Carton
JMT40KH18T1AC	JMT40KH18T1AC	T1A	100±5g/PCS	10 PCS	120 PCS

Typical Electrical & Thermal Characteristics

FIG.1: Power dissipation vs. on-state current
(per thyristor or diode)

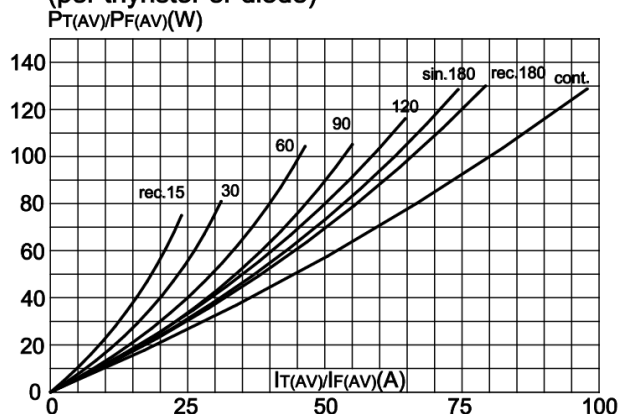


FIG.2: Maximum transient thermal impedance
junction to case(per thyristor or diode)

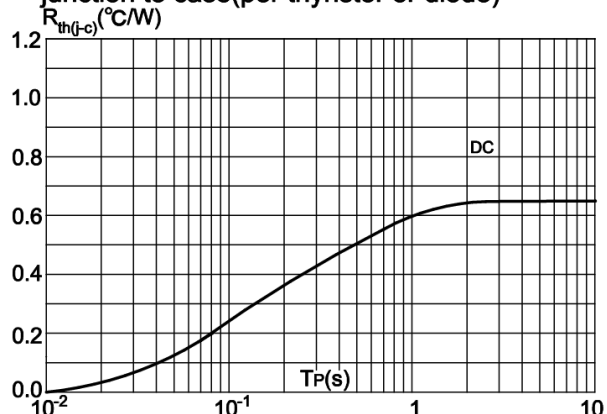


FIG.3: Forward characteristics
(per thyristor or diode)

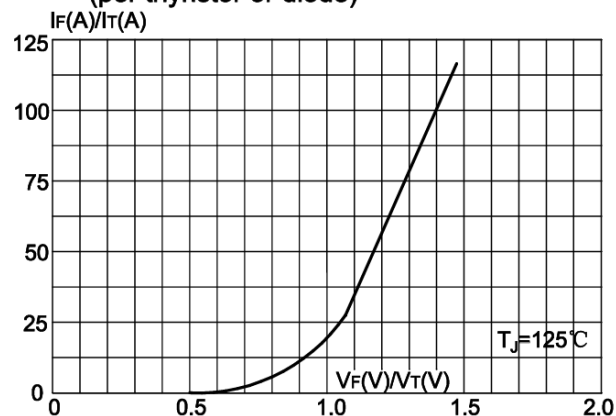


FIG.4: Relative variations of gate trigger current, holding current and latching current versus junction temperature

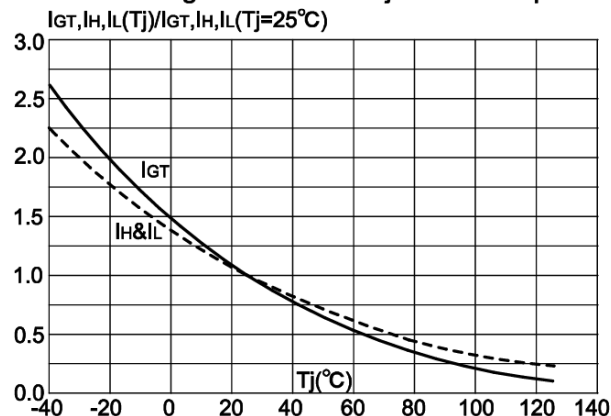


FIG.5 Gate trigger characteristics

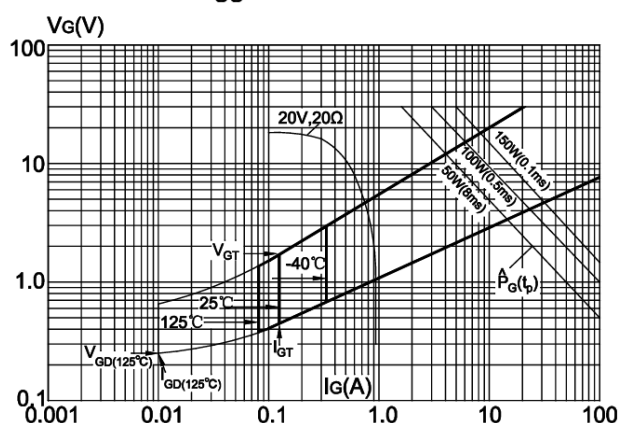
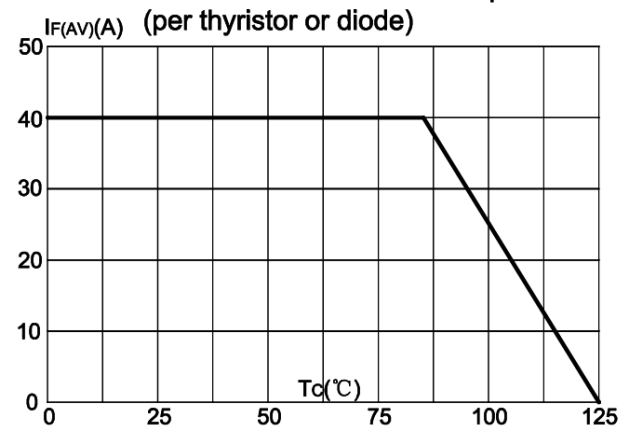
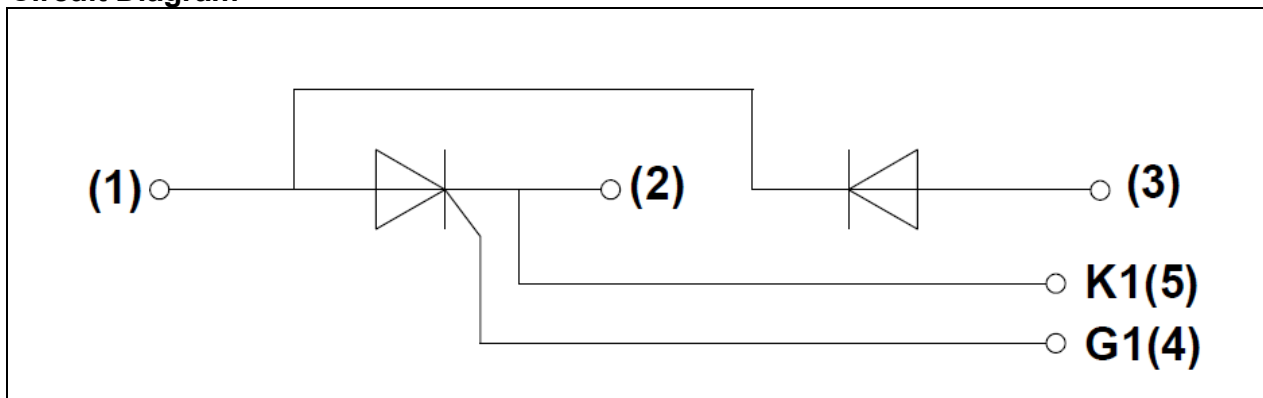


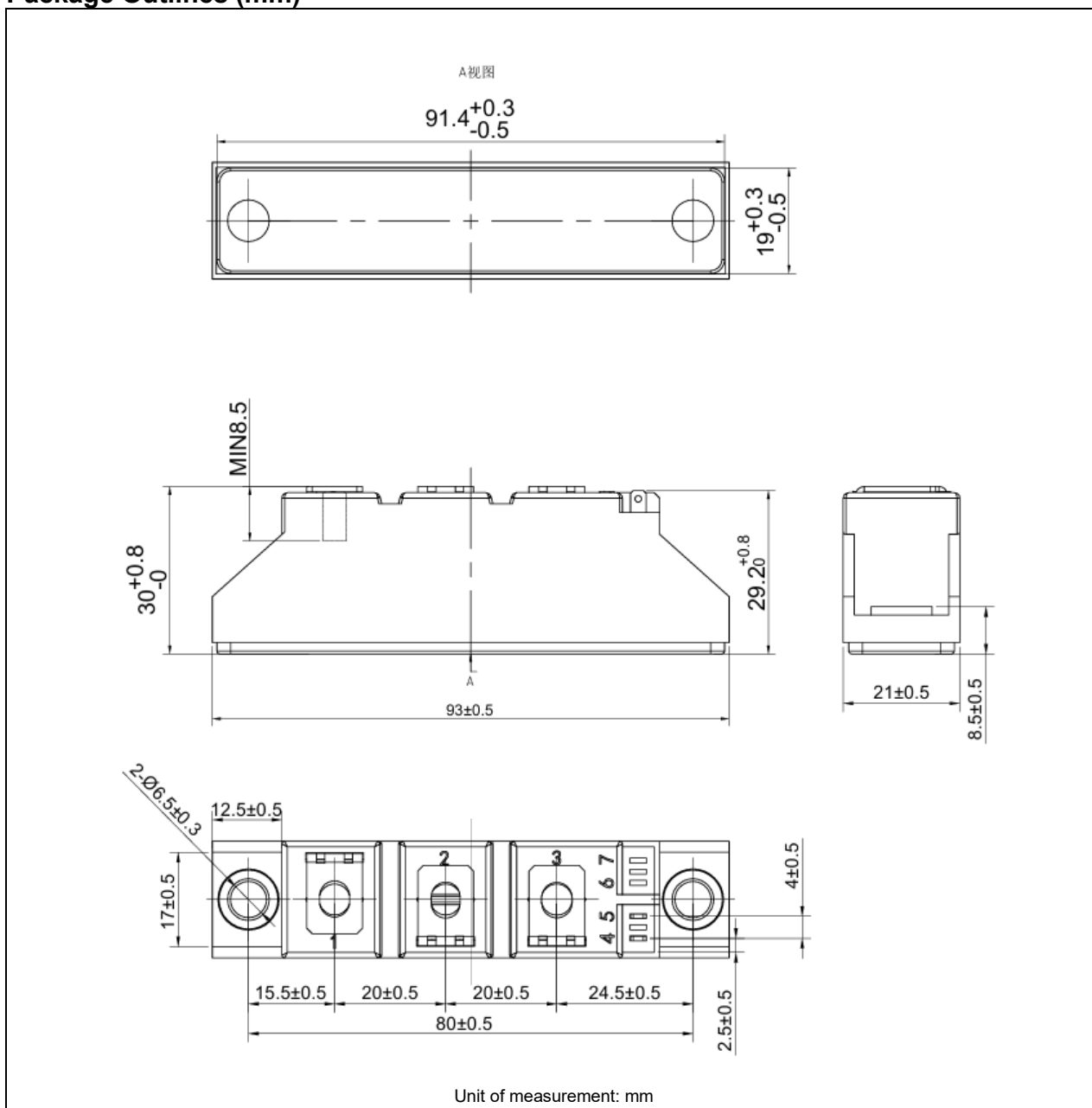
FIG.6: Forward current vs. case temperature



Circuit Diagram



Package Outlines (mm)





Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Semiconductor Co., Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it. This information in this document is subject to change without prior notice. Notwithstanding this, Jiangsu JieJie will fully comply with the terms outlined in a signed agreement. Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information. This document is the initial release, dated 14 August 2026. This document supersedes and replaces all information previously supplied.

 is registered trademark of Jiangsu JieJie Semiconductor Co., Lt ©2026 Jiangsu JieJie Semiconductor Co., Ltd. All rights reserved.